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OpenSFF Compute Node Specification 26.0.0DRAFT2

1. Introduction

1.1 Purpose

This document defines the OpenSFF specification for interoperable compute nodes. These standards enable modular, small form factor computing solutions across desktop workstations, all-in-one systems, and data center servers. This specification promotes an ecosystem of compatible components, innovation, and flexible system design.

1.2 Scope

This document defines the mechanical, electrical, and thermal characteristics of OpenSFF compute nodes. It covers the following aspects:

- Form factor and dimensions
- Mounting interface
- Connector placement and specifications (Core connector and Enterprise connector; see Section 2)
- Electrical power requirements
- Thermal design considerations for passive cooling
- Compliance and certification requirements

It applies to compute nodes that support a range of processors, from low-power solutions like the Intel N100 to high-performance APUs like the AMD Strix Halo. It defines requirements for both desktop and server variants of the compute node.

Note: The OpenSFF Enclosure Standards document provides additional specifications for enclosures that house OpenSFF compute nodes, and should be used in conjunction with this document.

1.3 Terminology and Abbreviations

- 4C+: Protocol-agnostic multi-lane high-speed connector with 168 contacts
- 4C: Protocol-agnostic multi-lane high-speed connector with 140 contacts
- APU: Accelerated Processing Unit
- EMC: Electromagnetic Compatibility
- EMI: Electromagnetic Interference
- TDP: Thermal Design Power
- VRM: Voltage Regulator Module
- SMT: Surface Mount Technology
- PCB: Printed Circuit Board
- DIMM: Dual In-line Memory Module
- CAMM: Compression Attached Memory Module
- NVMe: Non-Volatile Memory Express
- USB: Universal Serial Bus
- M.2: A form factor for solid-state drives
- I/O: Input/Output

1.4 Document Conventions

- All measurements and numeric values shall include their associated units.
- Requirements: The words "SHALL," "MUST," "SHOULD," and similar terms are used to indicate the relative degree of obligation in accordance with accepted standards practices as described in RFC 2119. See examples:

- "SHALL" or "MUST" indicate a mandatory requirement.
- "SHOULD" indicate a recommendation.
- "MAY" indicate that something is permissible.

1.5 Versioning Guidelines

The full version of any OpenSFF standard MUST follow the format “Year.Major.Minor.STAGE#”. This consists of:

- Year: The two-digit year in which the specification cycle began (e.g., 26 indicates the 2026 revision cycle). The Year field reflects a new generation of the standard that introduces substantial design or performance changes across the ecosystem.
- Major: Incremented when a change or clarification may affect product implementation.
- Minor: Incremented for editorial or non-technical changes that do not affect product implementation, including non-breaking corrections or clarifications made after an official version is released.
- STAGE#: An optional field that indicates the document’s development status, along with a number denoting revisions within the stage. These stages are:
  - DRAFT#: An internal working draft for development and early review
  - RC#: Release candidate, with completed content and published for public or partner review
  - (no suffix): Final release of a version

2. Compute Node Overview

OpenSFF provides a basis for building fully-featured systems for desktops and servers. The standard defines physical dimensions, electrical interface requirements, airflow, and other aspects that ensures the best possible compatibility between nodes and enclosures following the OpenSFF specification.

In all cases, this standard aims to specify only the minimum required details necessary and not interfere with the manufacturer’s ability to innovate and differentiate. Specifically, the following implementation details SHALL NOT be part of an OpenSFF standard:

- Manufacturer or distributor of components used
- Layout of components on the OpenSFF-compatible PCB as long as they reside entirely within the maximum dimensions set forth in this document
- Number and arrangement of additional I/O capabilities on the node’s I/O shield

To help with flexibility and reduce cost, the OpenSFF standard defines two node variants: Core and Enterprise. Both variants are designed to be interoperable, however, server features will only be accessible if both the node and the enclosure adhere to the Enterprise variant of the standard.

2.1 Core Features

Compute nodes following the Core variant are designed to feature a single SFF-TA-1002 4C+ connector (hereafter referred to as the Core connector). The pin assignments are not compatible with other standards like OCP NIC 3.0 that use the same connector.

The following signals are included on the Core connector:

- Two Ethernet ports, 2.5Gb or faster, named F1 and B1
- One DP 1.4 port or newer
- Power Button
- Reset Button
- Two USB 2.0 ports

- One USB-C port (24-pin connector), supporting at least USB 3.0 speeds
- One USB 3.0 Type A port

Notes:

The USB 3.0 Type A signal pin configuration MAY be used for external connectivity for Core enclosures. Additional external connectivity MAY also be provided by manufacturers via the I/O shield.

2.2 Enterprise Features

Compute nodes following the Enterprise variant of this standard MUST implement the Core connector as set forth in Section 2.1 with the same minimum capabilities.

Additionally, an Enterprise connector (SFF-TA-1002 4C) is used for the following signals:

- Two Ethernet ports, 2.5Gb or faster, named F2 and B2
- One USB-C port (24-pin connector), supporting at least USB 3.0 speeds

Notes:

The USB 3.0 Type-A signal referenced in Section 2.1 MUST be routed to an Ethernet-over-USB interface, which connects to the management module through an internal switch. This enables communication between the compute nodes and the management module.

Similar to Core nodes, manufacturers MAY optionally provide additional external connectivity for Enterprise variants through the I/O shield.

3. Physical Characteristics

This section details the physical characteristics and mechanical specifications for the compute node. Adherence to these guidelines ensures proper fit, function, and compatibility within the OpenSFF ecosystem.

3.1 Overall Compute Node Dimensions

The compute node MUST conform to the following overall dimensions, including the cooling shroud and I/O shield:

Parameter	Value	Notes
Length	215 mm	Measured from the inside mating surface of the I/O shield to the end of the connector plug
Width	150 mm	Full width of the I/O shield
Height (Total)	60 mm	Includes PCB, components, and cooling shroud

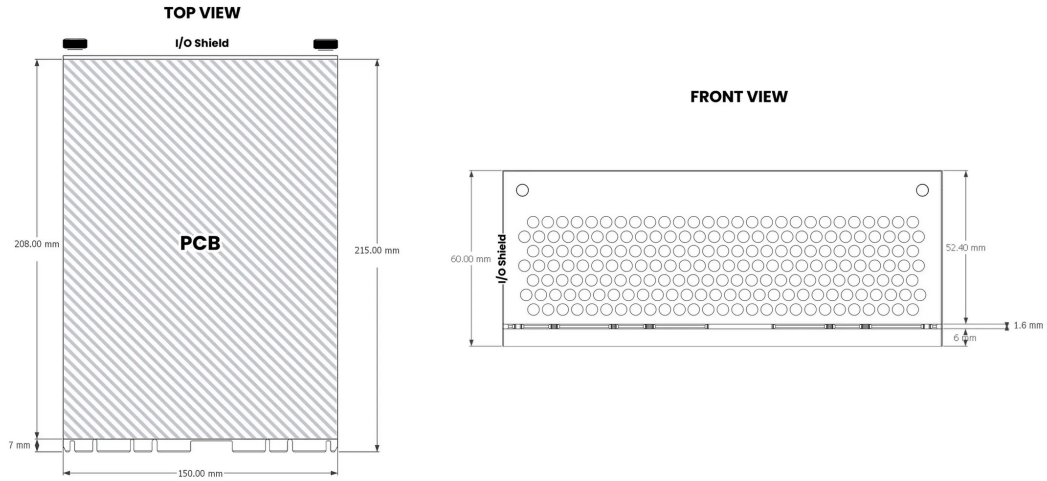

FIGURE 3.1. Compute node dimensions

3.2 Component Placement and Keep-Out Zones

This section defines the permissible dimensions for components on the PCB and areas where components MUST NOT be placed.

3.2.1 Top Components

The top side of the compute node PCB is typically populated with the following components:

- CPU and thermal solution
- Memory (SODIMM/CAMM/on-board)
- Voltage Regulator Modules (VRMs) and chokes
- M.2 slots and NVMe drives
- Other Surface Mount Devices (SMDs)

Maximum Dimensions for Components on the Top Side of the PCB:

- Length: 202 mm (centered): Maximum usable length, excluding the physical Core/Enterprise connector plug, accounting for keep-out zones along the PCB edges facing the edge plug and the I/O shield.
- Width: 140 mm (centered): Maximum usable width, allowing clearance for the PCB card support guides (see Section 3.5) and the air shroud (see Section 6.3).
- Height: 50 mm: Maximum height, considering PCB thickness and internal shroud height (see Section 6.3).

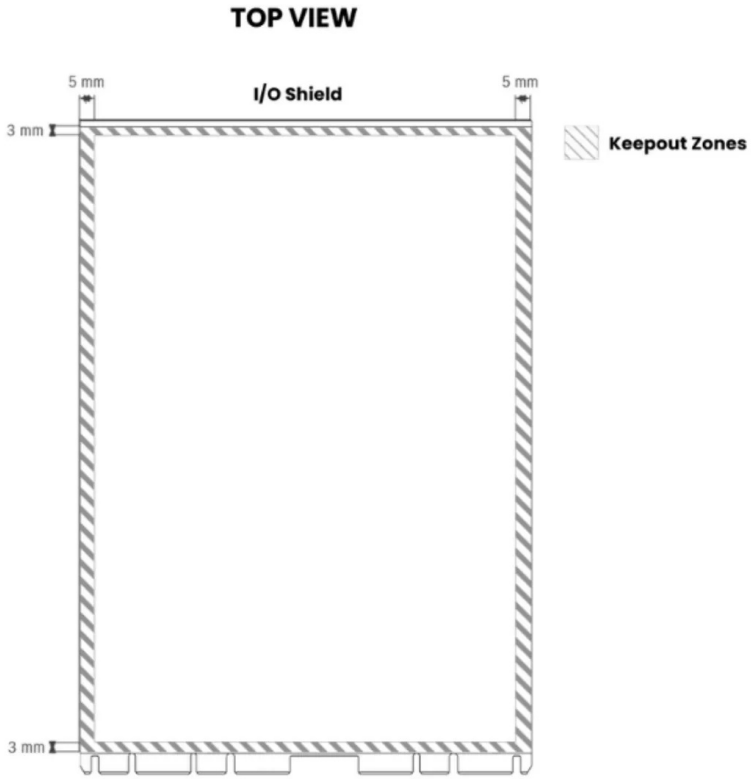

FIGURE 3.2.1 Keepout zones for top side components

3.2.2 Bottom Components

The underside of the compute node PCB is typically populated with the following components:

- Thermal solution backplates
- M.2 slots and drives
- Other Surface Mount Devices (SMDs)

The maximum dimensions of the components under the PCB MUST NOT exceed:

- Length: 202 mm (centered): Maximum usable length, excluding the physical Core/Enterprise connector plug, accounting for keep-out zones along the PCB edges facing the edge plug and the I/O shield.
- Width: 142 mm (centered): Maximum usable width, allowing clearance for the PCB card support guides
- Height: 6 mm

Components requiring consistent active or robust passive cooling (e.g., high-performance NVMe SSDs) are generally NOT recommended for placement on the bottom of the PCB due to limited airflow. Designers must ensure adequate thermal management for any heat-generating components in this area.

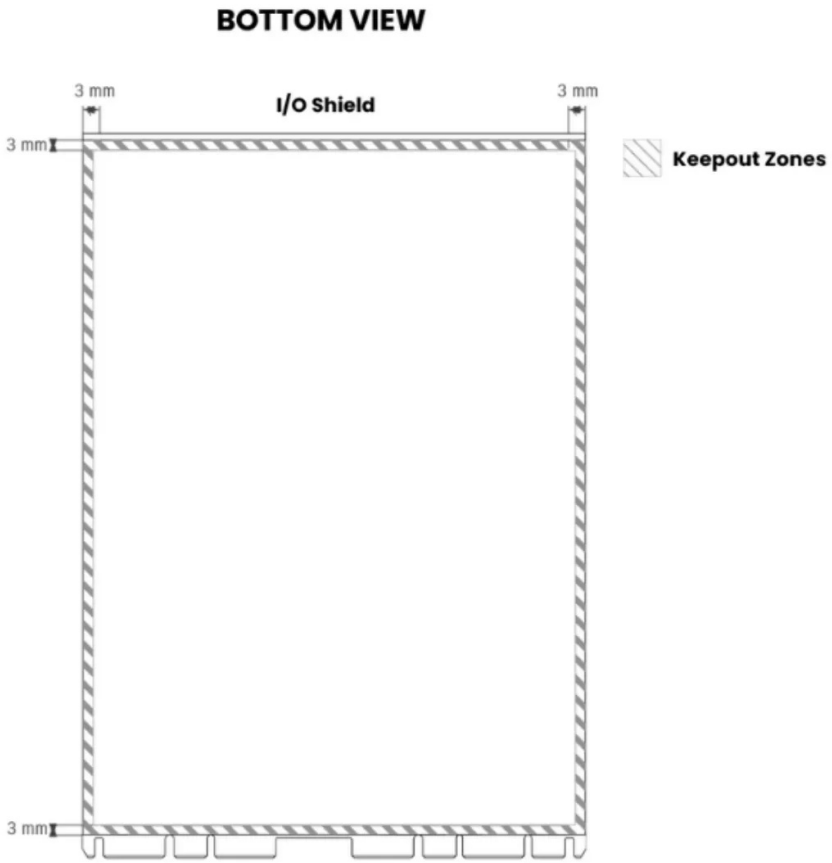

FIGURE 3.2.2 Keepout zones for components under the PCB

3.2.3 General Component Placement Restrictions

Component placement on both the top and bottom of the PCB MUST be restricted in the following areas:

- Length: To accommodate keep-out zones from the I/O shield and edge plug.
- Width: To allow space for the PCB card support guides and the node’s air shroud (top side only)
- Height: To allow easy insertion and removal and avoid interference with other enclosure components.

3.3 I/O Shield

The compute node MUST include a metal I/O shield to act as physical protection, airflow egress, electromagnetic interference (EMI) shielding, access to optional external connectors, and a mounting solution.

The I/O shield MUST have the following dimensions:

- Width: 150 mm
- Height: 60 mm
- Thickness: 1.2 mm (minimum)

The I/O shield MUST be perforated, to act as an exhaust for the node's cooling system.

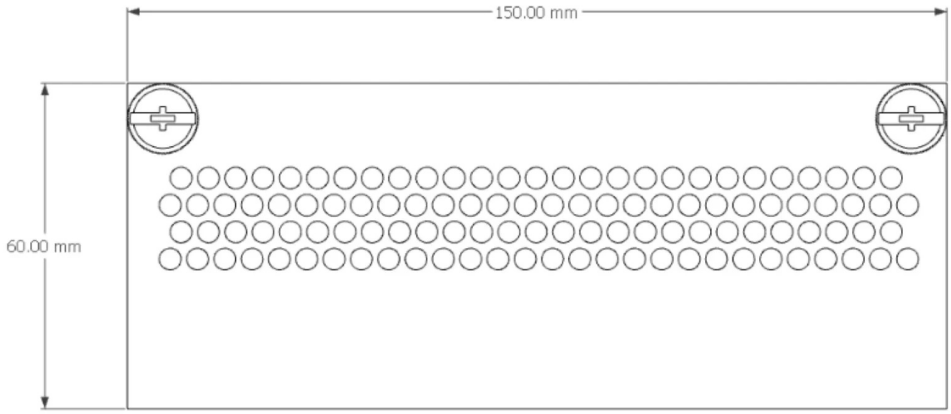

FIGURE 3.3.1. I/O shield dimensions

The I/O shield MUST be mounted using two captive M4 thumbscrews and matching screw holes, with the following specifications: /

- Mounting: Two captive M4 thumbscrews.
- Hole Center Location: 6.5 mm from top and side edges of the I/O shield.
- Screw Hole Clearance: Minimum 2.5 mm clearance around the screw hole (measured at the inside mating surface of the I/O shield).

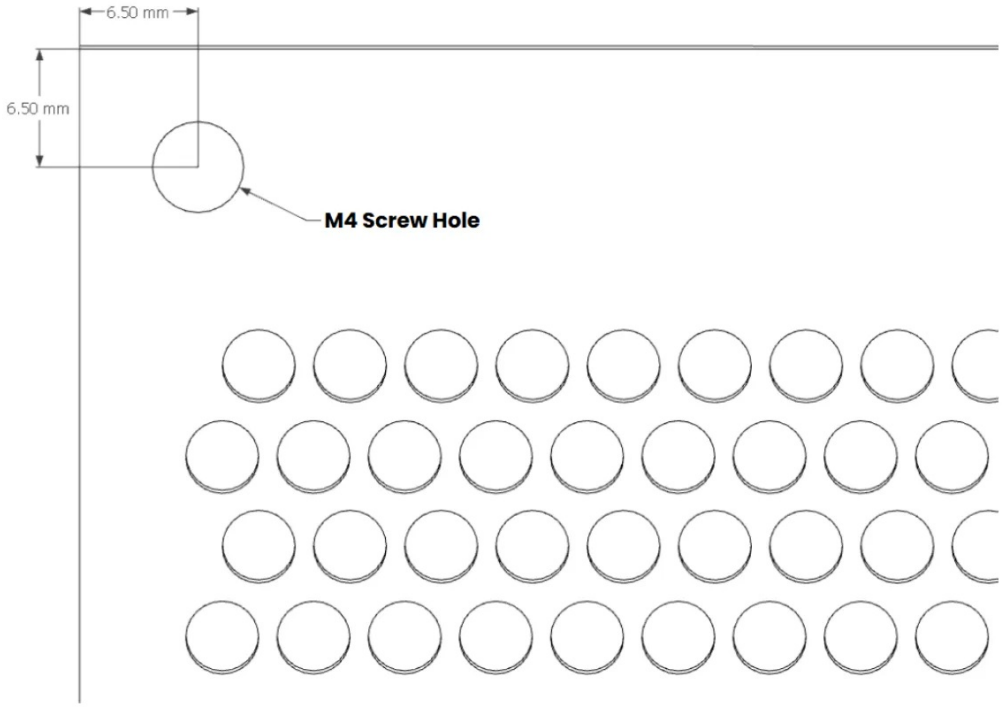

FIGURE 3.3.2. M4 screw hole position (only left side shown)

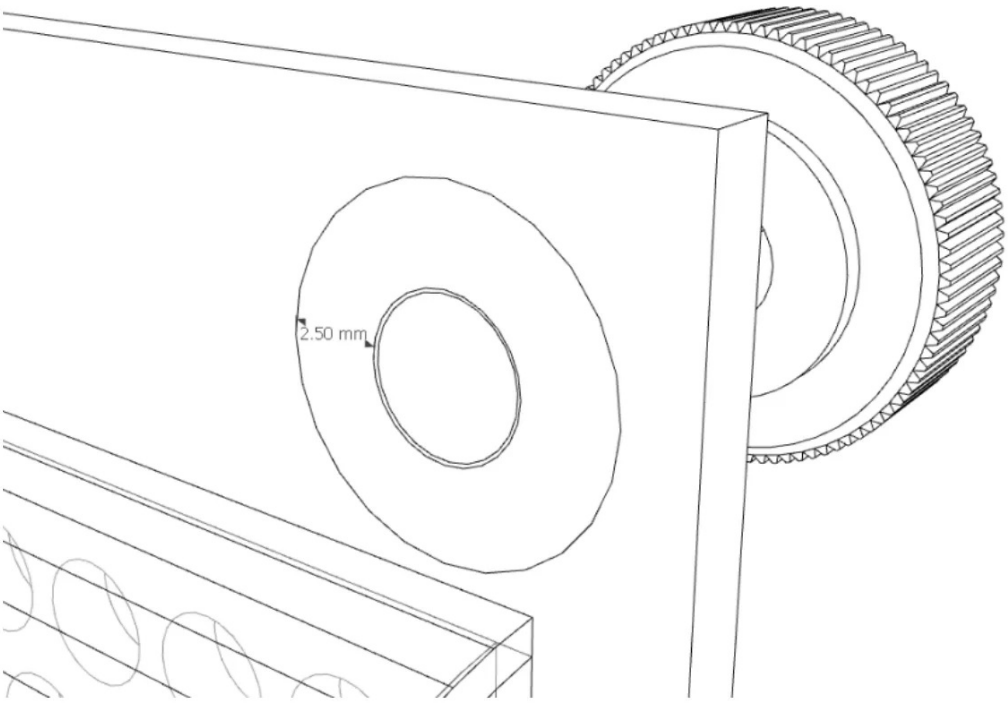

FIGURE 3.3.3. Screw hole clearance from inside mating surface of I/O shield

Additional connectors on the I/O shield may be connected at the manufacturer's discretion.

3.4 Mechanical Envelope and Retention Interface

OpenSFF compute nodes are designed for blind-mate insertion into compatible enclosure slots. This section defines the required mechanical envelope, rear connector alignment, and retention mechanism to ensure consistent fit and serviceability across OpenSFF enclosures.

3.4.1 Connector Alignment Plane

The compute node’s connectors are designed for blind-mate insertion into an enclosure-defined node bay envelope, which establishes the physical reference for connector positioning.

Connector alignment MUST comply with the following:

- The Core connector (4C+) MUST be positioned such that its outermost guide notch is exactly at the right edge of the I/O shield envelope (as viewed from the rear)
- If present, the Enterprise connector (4C) MUST be positioned such that its outermost guide notch is exactly at the left edge of the I/O shield envelope
- The horizontal distance between the inner faces of the two connectors (excluding guide notches) MUST be 22.73 mm
- Both connectors MUST be co-planar for reliable blind-mate insertion

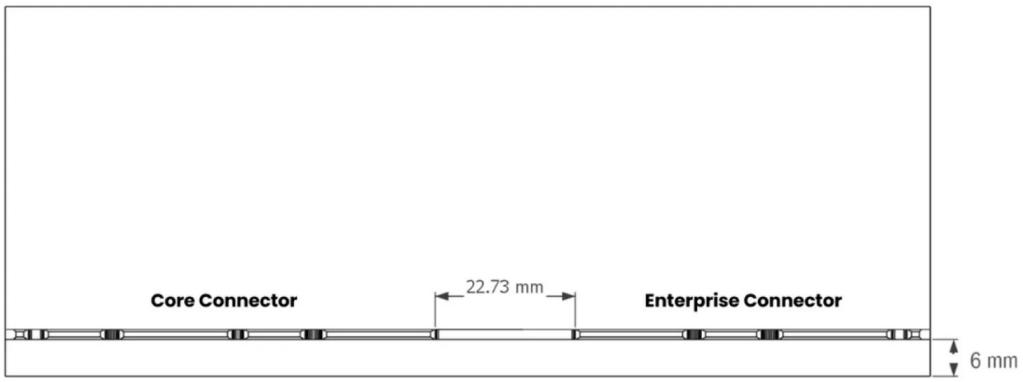

FIGURE 3.4.1 Core and Enterprise Plug Layout (Front View)

3.4.2 Enclosure Retention Interface

The compute node is secured within the enclosure using two captive M4 thumbscrews integrated into its rear I/O shield, as specified in Section 3.3. The enclosure MUST provide compatible threaded mounting points that align with the screw hole positions and support tool-less installation.

Specifically, the enclosure MUST:

- Position threaded retention points to match the node’s 6.5 mm offset from the top and side edges of the I/O shield
- Provide a rigid backing structure to prevent flex during tightening or vibration during operation
- Maintain a 2.5 mm clearance radius around each mounting point to avoid interference with the cooling shroud
- Recess the screw mating surface by 1.2 mm from the enclosure's interior panel face to accommodate the I/O shield thickness and ensure flush contact during retention

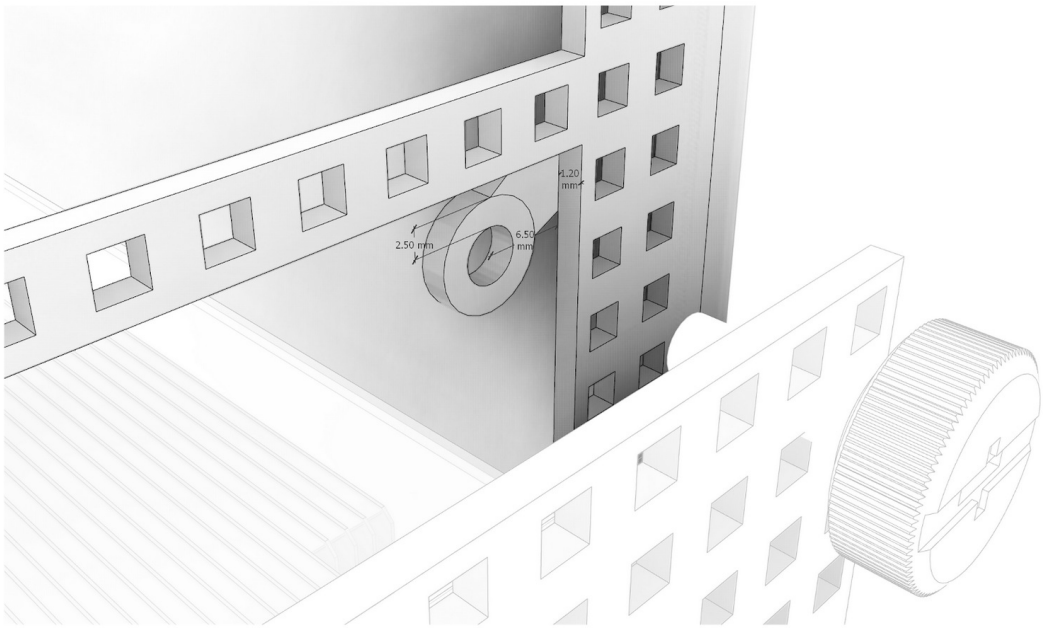

FIGURE 3.4.2 Node Retention Mechanism Layout and Measurements

3.5 PCB Guide Rail System

To ensure proper alignment, reduce connector wear, and support vibration and shock mitigation, compute nodes MUST accommodate enclosure-based PCB guide rails. This section defines the required interface clearances and alignment zones for compute node PCBs intended to operate such systems.

Specifications:

- The compute node PCB MUST reserve space for engagement with a dual vertical guide rail system provided by the enclosure.
- Two vertical guide rails SHALL be positioned parallel to the compute node's length axis, along the left and right edges of the PCB.
- The guide rails SHALL extend from the rear edge of the node (opposite the I/O shield) and MUST terminate no closer than 15 mm from the front face of the I/O shield.
- A minimum clearance zone of 3 mm MUST be maintained between the outer edge of the PCB and each guide rail (both sides).

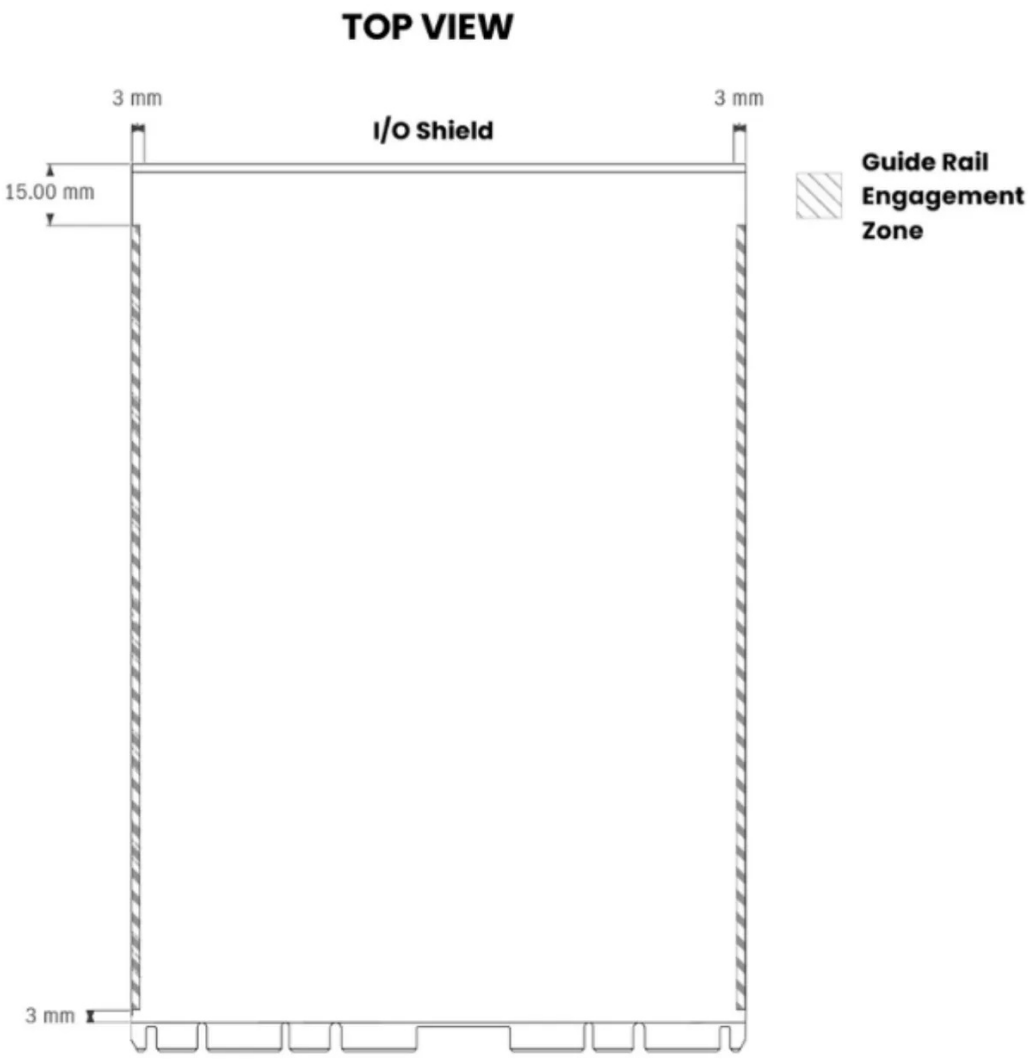

FIGURE 3.5 Guide Rail Engagement Zone

3.6 Temperature and Humidity Requirements

The compute node MUST be designed to operate within the following temperature and humidity ranges:

- Operating temperature: 10 °C to 35 °C
- Storage temperature: –40 °C to 65 °C
- Relative humidity: 8% to 80% (non-condensing)

3.7 Vibration Resistance

The compute node MUST be designed to withstand vibration levels encountered in typical operating environments. See section 7.3.1 for testing specifications.

3.8 Environmental Tolerance

Compute nodes MUST operate reliably in environments with typical indoor air quality, including the

presence of fine dust or particulate matter (PM5 or smaller), consistent with ISO 14644-1 Class 9 cleanliness levels. Nodes are NOT required to meet a formal Ingress Protection (IP) dust rating; however, they must exhibit baseline environmental resilience by withstanding standardized particulate exposure and durability validation tests. Designs SHALL NOT rely on user-replaceable air filters within the compute node itself to maintain operational integrity under these conditions.

Design considerations for dust resilience:

- All components critical to system operation (including CPU sockets, memory modules, VRMs, and the like) must be positioned to limit direct accumulation of non-conductive dust
- The shroud and its airflow pathways should be designed to reduce turbulence and stagnation zones where debris can accumulate
- Where feasible, PCB coatings MAY be used to mitigate the effects of inductive or corrosive dust ingress

Serviceability Guidelines:

- Compute nodes must be field-serviceable using non-specialized tools, with no requirement for internal cleaning during the expected lifecycle or warranty period (defined by vendor/manufacturing partner, not less than 3 years).
- Accessible areas (e.g. DIMM slots, M.2 storage slots) must remain free of obstructive debris that could impact upgrade or maintenance operations.

See section 7.2.7 for the testing requirements for dust/debris ingress.

4. Electrical Specifications

4.1 Connector Layout

The connector layout for the compute node MUST be as follows:

- Core Connector
  - Position: 0 mm from the left side of the system board (with plug connectors facing towards)
  - Guide notch location: On each side of the connector plug for Core variants. For Enterprise variants, only on the outer edge (away from the Enterprise Connector).
- Enterprise Connector (Enterprise node only)
  - Position: 0 mm from the right side of the system board
  - Guide notch location: The Enterprise connector’s notch must start flush with the rightmost side of the board.
- Spacing: 22.73 mm between the Core Connector and Enterprise Connector (if present)
- Inner Latches: If both connectors are used, no guide notches should be present on their inner sides (the sides facing each other).

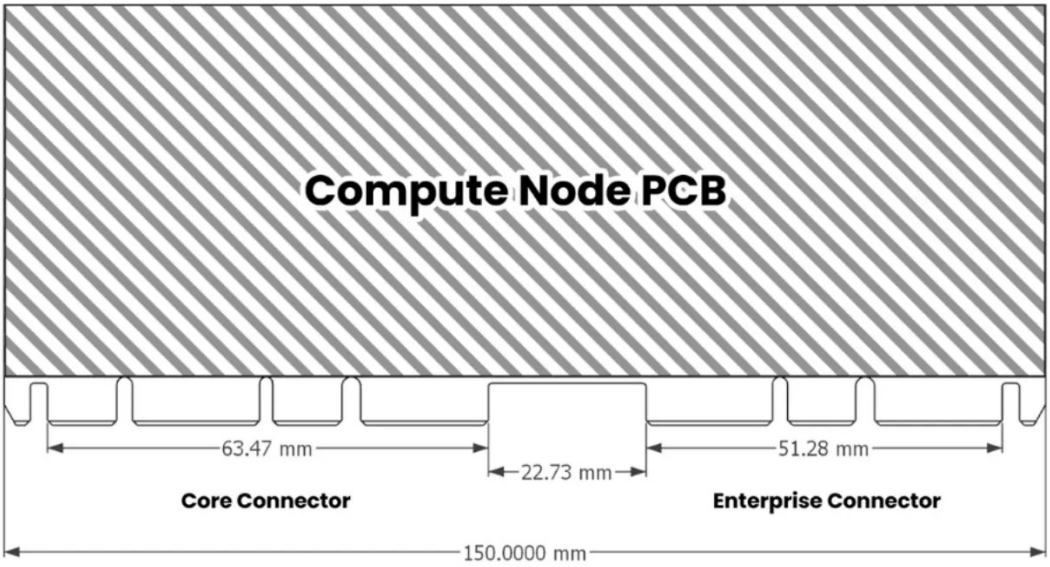

FIGURE 4.1. Core and Enterprise Connector Plug Layout on PCB

4.2 Power Requirements

- The compute node MUST be powered by 12 VDC through the Core connector.
- The compute node MUST support a maximum power consumption of 120 Watts.

4.3 Ethernet

The compute node MUST support Ethernet connectivity as follows:

- Number of ports: Two ports through the Core connector and an additional two ports through the Enterprise connector
- Speed: 2.5 Gbps
- Connector type: RJ-45

4.4 USB

The compute node MUST support USB connectivity as follows:

- Number of USB 2.0 ports: Two
- Number of USB-C ports: One port through the Core connector and an additional port through the Enterprise connector, supporting at least USB 3.0 speeds
- Number of USB 3.0 ports: One allocation for a Type A connector for external use or as an interface for node and management communication over Ethernet (mentioned in Sections 2.1 and 2.2).

4.5 DisplayPort

- The compute node MUST support DisplayPort connectivity with a minimum version of 1.4.

4.6 Front Panel Connectors

The compute node MUST provide connectors for front panel functionality, including:

- Power button
- Reset button
- Front panel audio (stereo line out and mic)

5. Connector Specifications

5.1 4C+ Connector (Core)

General Description: The 4C+ connector, referred to in this specification as the Core connector, is a card edge interface based on the SFF-TA-1002 specification. It is used in both Core and Enterprise compute nodes, and features 168 contacts and supports up to 52 differential pairs of high-speed signals.

5.1.1 Pin Assignment

The 4C+ connector used in OpenSFF compute nodes follows a standardized pin configuration optimized for signal integrity, interoperability, and power distribution. The layout includes:

- Predefined ground pins distributed throughout the connector to minimize impedance and improve return path quality
- Dedicated power and management pins, which MUST NOT be reassigned for signaling purposes
- High-speed signal lanes arranged in a GSSGSSG pattern to support clean differential pair routing and minimize crosstalk

Both Core and Enterprise variants of the OpenSFF compute node MUST use the 4C+ pinouts as specified in Figure 5.1.1.

Primary Connector (4C+)					
Side A			Side B		
Pin #	Signal	Description	Pin #	Signal	Description
OA1	+12V	+12 volt power	OB1	+12V	+12 volt power
OA2	+12V	+12 volt power	OB2	+12V	+12 volt power
OA3	+12V	+12 volt power	OB3	+12V	+12 volt power
OA4	+12V	+12 volt power	OB4	+12V	+12 volt power
OA5	+12V	+12 volt power	OB5	+12V	+12 volt power
OA6	+12V	+12 volt power	OB6	+12V	+12 volt power
OA7	+12V	+12 volt power	OB7	+12V	+12 volt power
OA8	+12V	+12 volt power	OB8	+12V	+12 volt power
OA9	GND	Ground	OB9	GND	Ground
OA10	res	Reserved	OB10	res	Reserved
OA11	res	Reserved	OB11	res	Reserved
OA12	GND	Ground	OB12	GND	Ground
OA13	res	Reserved	OB13	res	Reserved
OA14	res	Reserved	OB14	res	Reserved
KEY					
A1	FP_OUT_L	Left Channel Audio Signal to Front Panel	B1	POWER_BTN	Power button
A2	FP_OUT_R	Right Channel Audio Signal to Front Panel	B2	RESET	Reset signal
A3	AUD_GND	Ground for analog audio	B3	LED_STATUS	Front Panel Power LED
A4	MIC	Front Panel Mic Input	B4	FAN_PWM	Fan Control
A5	res	Reserved	B5	res	Reserved
A6	res	Reserved	B6	res	Reserved
A7	GND	Ground	B7	GND	Ground
A8	USB0_D+	USB-A 3.0 Port 0 Data+	B8	USB1_D+	USB-A 3.0 Port 1 Data+
A9	USB0_D-	USB-A 3.0 Port 0 Data-	B9	USB1_D-	USB-A 3.0 Port 1 Data-
A10	GND	Ground	B10	GND	Ground
A11	USB3_0_SSTXp2	USB-A 3.0 Port 0 SS Transmit Data+	B11	USB3_1_SSTXp2	USB-A 3.0 Port 1 SS Transmit Data+
A12	USB3_0_SSTXn2	USB-A 3.0 Port 0 SS Transmit Data-	B12	USB3_1_SSTXn2	USB-A 3.0 Port 1 SS Transmit Data-
A13	GND	Ground	B13	GND	Ground
A14	USB3_0_SSRXp2	USB-A 3.0 Port 0 SS Receive Data+	B14	USB3_1_SSRXp2	USB-A 3.0 Port 1 SS Receive Data+
A15	USB3_0_SSRXn2	USB-A 3.0 Port 0 SS Receive Data-	B15	USB3_1_SSRXn2	USB-A 3.0 Port 1 SS Receive Data-
A16	GND	Ground	B16	GND	Ground
A17	ETH0_BI+_D3	Ethernet Port 0 Bi-directional+ (Pair 1)	B17	ETH0_TX+_D1	Ethernet Port 0 Transmit Data+ (Pair 2)
A18	ETH0_BI-_D3	Ethernet Port 0 Bi-directional- (Pair 1)	B18	ETH0_TX-_D1	Ethernet Port 0 Transmit Data- (Pair 2)
A19	GND	Ground	B19	GND	Ground
A20	ETH0_RX+_D2	Ethernet Port 0 Receive Data+ (Pair 3)	B20	ETH0_BI+_D4	Ethernet Port 0 Bi-directional+ (Pair 4)
A21	ETH0_RX-_D2	Ethernet Port 0 Receive Data- (Pair 3)	B21	ETH0_BI-_D4	Ethernet Port 0 Bi-directional- (Pair 4)
A22	GND	Ground	B22	GND	Ground
A23	ETH1_BI+_D3	Ethernet Port 1 Bi-directional+ (Pair 1)	B17	ETH1_TX+_D1	Ethernet Port 1 Transmit Data+ (Pair 2)
A24	ETH1_BI-_D3	Ethernet Port 1 Bi-directional- (Pair 1)	B18	ETH1_TX-_D1	Ethernet Port 1 Transmit Data- (Pair 2)
A25	GND	Ground	B19	GND	Ground
A26	ETH1_RX+_D2	Ethernet Port 1 Receive Data+ (Pair 3)	B20	ETH1_BI+_D4	Ethernet Port 1 Bi-directional+ (Pair 4)
A27	ETH1_RX-_D2	Ethernet Port 1 Receive Data- (Pair 3)	B21	ETH1_BI-_D4	Ethernet Port 1 Bi-directional- (Pair 4)
A28	GND	Ground	B28	GND	Ground
KEY					
A29	GND	Ground	B29	GND	Ground
A30	USBC0_SSTXp1	USB-C Port 0 SS Transmit Data+ (Pair 1)	B30	USBC0_SSRXp1	USB-C Port 0 SS Receive Data+ (Pair 2)
A31	USBC0_SSTXn1	USB-C Port 0 SS Transmit Data+ (Pair 1)	B31	USBC0_SSRXn1	USB-C Port 0 SS Receive Data- (Pair 2)
A32	GND	Ground	B32	GND	Ground
A33	USBC0_SSTXp2	USB-C Port 0 SS Transmit Data+ (Pair 3)	B33	USBC0_SSRXp2	USB-C Port 0 SS Receive Data+ (Pair 4)

A34	USBC0_SSTXn2	USB-C Port 0 SS Transmit Data+ (Pair 3)	B34	USBC0_SSRXn2	USB-C Port 0 SS Receive Data+ (Pair 4)
A35	GND	Ground	B35	GND	Ground
A36	USBC0_Dp1	USB-C Port 0 USB 2.0 Data+ (Pair 1)	B36	USBC0_Dp2	USB-C Port 0 USB 2.0 Data+ (Pair 2)
A37	USBC0_Dn1	USB-C Port 0 USB 2.0 Data- (Pair 1)	B37	USBC0_Dn2	USB-C Port 0 USB 2.0 Data- (Pair 2)
A38	GND	Ground	B38	GND	Ground
A39	USBC0_SBU1	USB-C Port 0 Sideband Use 1	B39	USBC0_SBU2	USB-C Port 0 Sideband Use 2
A40	USBC0_CC1	USB-C Port 0 Configuration Channel 2	B40	USBC0_CC2	USB-C Port 0 Configuration Channel 2
A41	GND	Ground	B41	GND	Ground
A42	NODE_PRESENT	Node present (Either core or Ent)	B42	ENTERPRISE	GND on enterprise, pull up in core
KEY					
A43	GND	Ground	B43	GND	Ground
A44	DP_ML_Lane_p0	Displayport Main Link Lane+ (Pair 1)	B44	DP_ML_Lane_p1	Displayport Main Link Lane+ (Pair 2)
A45	DP_ML_Lane_n0	Displayport Main Link Lane- (Pair 1)	B45	DP_ML_Lane_n1	Displayport Main Link Lane- (Pair 2)
A46	GND	Ground	B46	GND	Ground
A47	DP_ML_Lane_p2	Displayport Main Link Lane+ (Pair 3)	B47	DP_ML_Lane_p3	Displayport Main Link Lane+ (Pair 4)
A48	DP_ML_Lane_n2	Displayport Main Link Lane- (Pair 3)	B48	DP_ML_Lane_n3	Displayport Main Link Lane- (Pair 4)
A49	GND	Ground	B49	GND	Ground
A50	DP_AUXCH_p	Displayport Auxiliary Channel+	B50	DP_HOTPLUG	Displayport Hot Plug Detect
A51	DP_AUXCH_n	Displayport Auxiliary Channel-	B51	res	Reserved
A52	GND	Ground	B52	GND	Ground
A53	USB1_D+	USB 2.0 Port 1 Data+	B53	USB2_D+	USB 2.0 Port 2 Data+
A54	USB1_D-	USB 2.0 Port 1 Data-	B54	USB2_D-	USB 2.0 Port 2 Data-
A55	GND	Ground	B55	GND	Ground
A56	res	Reserved	B56	res	Reserved
A57	res	Reserved	B57	res	Reserved
A58	GND	Ground	B58	GND	Ground
A59	res	Reserved	B59	res	Reserved
A60	res	Reserved	B60	res	Reserved
A61	GND	Ground	B61	GND	Ground
A62	res	Reserved	B62	res	Reserved
A63	res	Reserved	B63	res	Reserved
A64	GND	Ground	B64	GND	Ground
A65	res	Reserved	B65	res	Reserved
A66	res	Reserved	B66	res	Reserved
A67	GND	Ground	B67	GND	Ground
A68	res	Reserved	B68	res	Reserved
A69	+12V	+12 volt power	B69	+12V	+12 volt power
A70	+12V	+12 volt power	B70	+12V	+12 volt power

FIGURE 5.1.1. Core Connector Pinout

Note: Reserved pins MAY be used by manufacturers to add features to the compute node, such as additional I/O ports.

5.1.2 Supported Protocols

The 4C+ connector is designed for multi-protocol operation and supports simultaneous use of:

- PCIe Gen 3 / 4 / 5 / 6
- Ethernet
- USB 2.0 / USB 3.x / USB4
- DisplayPort 1.4 or newer
- I2C / SMBus / Sideband signals
- NVMe, SATA, SAS (depending on system design)

5.1.3 Electrical Characteristics

Key electrical parameters of the 4C+ connector are as follows:

- Signaling Rate: Up to 112 GT/s PAM4
- Impedance: This specification does not restrict, require or define a specific impedance for the connector.
- Voltage / Current Ratings:
    - Max voltage: 12 VDC

    - Max current: 1.1 A per power contact, 0.5 A per signal contact
    - Temperature rating: –40 °C to 85 °C
- Power Integrity:
    - The connector includes an internally linked ground network that provides a low-inductance, low-impedance return path for high-speed signals.

5.1.4 Mechanical Characteristics

- Mating Style: Card edge
- Mating Cycles:
    - ≥ 200 (Grade 2 durability)
    - Connector wipe length: 0.40 mm (Gold-Gold interface)
- Mounting Type: Surface Mount Technology (SMT)
- Dimensions (Straddle Mount):
    - Width: 73 mm
    - Pitch: 0.60 mm
    - Height: 10.05 mm max
    - Compatible with host PCB thickness of 1.57±0.13 mm

5.2 4C Connector (Enterprise)

General Description: The 4C connector, referred to in this specification as the Enterprise connector, is used exclusively in Enterprise variant compute nodes. It is a card edge interface based on the SFF-TA-1002 specification. It features 140 contacts and supports up to 44 differential pairs of high-speed signals.

5.2.1 Pin Assignment

The 4C connector used in OpenSFF compute nodes follows a standardized pin configuration optimized for signal integrity and interoperability. The layout includes:

- High-speed signal lanes arranged in a GSSGSSG pattern to support clean differential pair routing and minimize crosstalk
- Predefined ground pins distributed throughout the connector to minimize impedance and improve return path quality

Enterprise variants of the OpenSFF compute node MUST use the 4C pinouts as specified in Figure 5.2.1.

Secondary Connector (4C / Enterprise Nodes only)					
Side A			Side B		
Pin #	Signal	Description	Pin #	Signal	Description
A1	GND	Ground	B1	GND	Ground
A2	res	Reserved	B2	res	Reserved
A3	res	Reserved	B3	res	Reserved
A4	GND	Ground	B4	GND	Ground
A5	res	Reserved	B5	res	Reserved
A6	res	Reserved	B6	res	Reserved
A7	GND	Ground	B7	GND	Ground
A8	res	Reserved	B8	res	Reserved
A9	res	Reserved	B9	res	Reserved

A10	GND	Ground	B10	GND	Ground
A11	res	Reserved	B11	res	Reserved
A12	res	Reserved	B12	res	Reserved
A13	GND	Ground	B13	GND	Ground
A14	res	Reserved	B14	res	Reserved
A15	res	Reserved	B15	res	Reserved
A16	GND	Ground	B16	GND	Ground
A17	ETH2_BI+_D3	Ethernet Port 2 Bi-directional+ (Pair 1)	B17	ETH2_TX+_D1	Ethernet Port 2 Transmit Data+ (Pair 2)
A18	ETH2_BI-_D3	Ethernet Port 2 Bi-directional- (Pair 1)	B18	ETH2_TX-_D1	Ethernet Port 2 Transmit Data- (Pair 2)
A19	GND	Ground	B19	GND	Ground
A20	ETH2_RX+_D2	Ethernet Port 2 Receive Data+ (Pair 3)	B20	ETH2_BI+_D4	Ethernet Port 2 Bi-directional+ (Pair 4)
A21	ETH2_RX-_D2	Ethernet Port 2 Receive Data- (Pair 3)	B21	ETH2_BI-_D4	Ethernet Port 2 Bi-directional- (Pair 4)
A22	GND	Ground	B22	GND	Ground
A23	ETH3_BI+_D3	Ethernet Port 3 Bi-directional+ (Pair 1)	B27	ETH3_TX+_D1	Ethernet Port 3 Transmit Data+ (Pair 2)
A24	ETH3_BI-_D3	Ethernet Port 3 Bi-directional- (Pair 1)	B28	ETH3_TX-_D1	Ethernet Port 3 Transmit Data- (Pair 2)
A25	GND	Ground	B29	GND	Ground
A26	ETH3_RX+_D2	Ethernet Port 3 Receive Data+ (Pair 3)	B20	ETH3_BI+_D4	Ethernet Port 3 Bi-directional+ (Pair 4)
A27	ETH3_RX-_D2	Ethernet Port 3 Receive Data- (Pair 3)	B21	ETH3_BI-_D4	Ethernet Port 3 Bi-directional- (Pair 4)
A28	GND	Ground	B28	GND	Ground
KEY					
A29	GND	Ground	B29	GND	Ground
A30	USBC1_SSTXp1	USB-C Port 1 SS Transmit Data+ (Pair 1)	B30	USBC1_SSRXp1	USB-C Port 1 SS Receive Data+ (Pair 2)
A31	USBC1_SSTXn1	USB-C Port 1 SS Transmit Data+ (Pair 1)	B31	USBC1_SSRXn1	USB-C Port 1 SS Receive Data- (Pair 2)
A32	GND	Ground	B32	GND	Ground
A33	USBC1_SSTXp2	USB-C Port 1 SS Transmit Data+ (Pair 3)	B33	USBC1_SSRXp2	USB-C Port 1 SS Receive Data+ (Pair 4)
A34	USBC1_SSTXn2	USB-C Port 1 SS Transmit Data+ (Pair 3)	B34	USBC1_SSRXn2	USB-C Port 1 SS Receive Data+ (Pair 4)
A35	GND	Ground	B35	GND	Ground
A36	USBC1_Dp1	USB-C Port 1 USB 2.0 Data+ (Pair 1)	B36	USBC1_Dp2	USB-C Port 1 USB 2.0 Data+ (Pair 2)
A37	USBC1_Dn1	USB-C Port 1 USB 2.0 Data- (Pair 1)	B37	USBC1_Dn2	USB-C Port 1 USB 2.0 Data- (Pair 2)
A38	GND	Ground	B38	GND	Ground
A39	USBC1_SBU1	USB-C Port 1 Sideband Use 1	B39	USBC1_SBU2	USB-C Port 1 Sideband Use 2
A40	USBC1_CC1	USB-C Port 1 Configuration Channel 2	B40	USBC1_CC2	USB-C Port 1 Configuration Channel 2
A41	GND	Ground	B41	GND	Ground
A42	res	Reserved	B42	res	Reserved
KEY					
A43	GND	Ground	B43	GND	Ground
A44	res	Reserved	B44	res	Reserved
A45	res	Reserved	B45	res	Reserved
A46	GND	Ground	B46	GND	Ground
A47	res	Reserved	B47	res	Reserved
A48	res	Reserved	B48	res	Reserved
A49	GND	Ground	B49	GND	Ground
A50	res	Reserved	B50	res	Reserved
A51	res	Reserved	B51	res	Reserved
A52	GND	Ground	B52	GND	Ground
A53	res	Reserved	B53	res	Reserved
A54	res	Reserved	B54	res	Reserved
A55	GND	Ground	B55	GND	Ground
A56	res	Reserved	B56	res	Reserved
A57	res	Reserved	B57	res	Reserved
A58	GND	Ground	B58	GND	Ground
A59	res	Reserved	B59	res	Reserved
A60	res	Reserved	B60	res	Reserved
A61	GND	Ground	B61	GND	Ground
A62	res	Reserved	B62	res	Reserved
A63	res	Reserved	B63	res	Reserved
A64	GND	Ground	B64	GND	Ground
A65	res	Reserved	B65	res	Reserved
A66	res	Reserved	B66	res	Reserved
A67	GND	Ground	B67	GND	Ground
A68	res	Reserved	B68	res	Reserved
A69	res	Reserved	B69	res	Reserved
A70	res	Reserved	B70	res	Reserved

Ground
USB
Ethernet
Reserved

FIGURE 5.2.1. Enterprise Connector Pinout

5.2.2 Supported Protocols

The 4C connector supports a variety of signaling protocols and sideband interfaces, including:

- PCIe Gen 3 / 4 / 5 / 6
- Ethernet
- USB 2.0 / USB 3.x / USB4

- DisplayPort 1.4 or newer
- I2C / SMBus / Sideband signals
- NVMe, SATA, SAS (depending on system design)

5.2.3 Electrical Characteristics

Key electrical parameters of the 4C+ connector are as follows:

- Signaling Rate: Up to 112 GT/s PAM4
- Impedance: This specification does not restrict, require or define a specific impedance for the connector.
- Voltage / Current Ratings:
  - Max voltage: 12 VDC
  - Max current: 1.1 A per power contact, 0.5 A per signal contact
  - Temperature rating: –40 °C to 85 °C
- Power Integrity:
  - The connector includes an internally linked ground network that provides a low-inductance, low-impedance return path for high-speed signals.

5.2.4 Mechanical Characteristics

- Mating Style: Card edge
- Mating Cycles:
  - ≥ 200 (Grade 2 durability)
  - Connector wipe length: 0.40 mm (Gold-Gold interface)
- Mounting Type: Surface Mount Technology (SMT)
- Dimensions (Straddle Mount):
  - Width: 60.8 mm
  - Pitch: 0.60 mm
  - Height: 10.05 mm max
  - Compatible with host PCB thickness of 1.57±0.13 mm

6. Airflow and Cooling

The compute node features front-to-back airflow, from intake fans that are part of the enclosure, through a plastic shroud that optimizes airflow, and out the perforations on the I/O shield. The node's major components are passively cooled through the node's thermal solution that MUST function as part of the active cooling setup provided by the enclosure.

6.1 Cooling Requirements

The cooling system must effectively manage thermal output across a range of inlet air temperatures, specifically from 10°C to 35°C. This includes ensuring that the CPU/APU die and memory module temperatures remain below a specified maximum junction temperature (Tj), to avoid thermal throttling and/or component damage.

- Maximum Ambient Temperature / Intake Temperature: 35°C
- Maximum Junction Temperature (CPU/APU Core): 85°C
- Maximum Junction Temperature (Memory Modules): 85°C
- Maximum VRM Mosfet Casing Temperature: 120°C

To ensure reliable thermal operation of compute nodes within the OpenSFF enclosure environment, the cooling system must deliver sufficient volumetric airflow across critical thermal components. The following airflow thresholds are defined:

- Minimum airflow requirement: The system must maintain a minimum of 68 m³/h of effective airflow across the primary thermal interface zones., measured at the shroud inlet.
- Required static pressure: The system must sustain a minimum static pressure of 11.943 mmH_2O at 68 m³/h to ensure that airflow is preserved through the node's thermal soulution (e.g, heatsink fins), ducting, filters, and any restrictive chassis features.

These figures are based on theoretical airflow calculations, but adjusted to 200% based on empirical data from comparable systems to ensure broader system compatibility.

6.2 Thermal Solution Design

Effective thermal management is critical to ensuring reliable operation and performance of the compute node. This section defines the requirements and guidelines for designing thermal solutions that keep all critical components within safe operating limits, while allowing flexibility in methods of implementation.

6.2.1 Mandatory Requirements

- The compute node MUST incorporate a thermal solution capable of keeping components within the temperature limits defined in Section 6.1, including but not limited to the CPU/APU, memory modules, and VRMs
- In designs where component power dissipation is sufficiently low (e.g., below 10 W TDP), a dedicated node-level thermal assembly MAY be omitted if the enclosure-provided airflow system maintains compliance within the limits defined in Section 6.1
- Where thermal conduction to a cooling assembly is required, high-quality Thermal Interface Material (TIM) or an equivalent solution MUST be applied
- The thermal solution MUST operate effectively in conjunction with the enclosure-provided airflow system as specified in Section 6.1.

6.2.2 Design Guidelines

- The thermal solution SHOULD be optimized for the enclosure's airflow path and pressure characteristics
- Acceptable methods include, but are not limited to heatsinks, vapor chambers, heatpipes, and other thermal transfer assemblies
- Configurations utilizing high-TDP components MAY require a thermal solution design that extends over surface-mounted memory (if applicable) and Voltage Regulator Modules (VRMs)
- Cutouts, pedestals, or equivalent design features MAY be used to minimize TIM bond-line thickness over designated components

6.2.3 Solution Specifications

- Maximum TDP Supported: 120W
- The solution's physical dimensions MUST comply with top-component height limits (see Section 3.2).

6.3 The Shroud

A shroud MUST be used to direct enclosure-provided airflow across the node's thermal solution and other heat-sensitive components. The shroud helps reduce airflow losses inside the enclosure and can protect components during handling.

- Maximum External Dimensions: 215mm (Length) x 144mm (Width) x 52.4mm (Height)
    - The top and side sections of the shroud's inlet MUST extend beyond PCB length by 7mm (same as the length of the plug) forming the inlet section, in order to create a seal against the enclosure's intake fan array.

    - The width and height of the shroud must be tapered at the top corners to ensure sufficient clearance for the screw holes of the I/O shield, allowing space for the thumb screw mounting posts of the enclosure (as shown in Figure 3.4.2).
- Shroud Inlet: Minimum inlet area of 40mm (H) x 96mm (W).
- Shroud Outlet: I/O shield perforations SHALL cover the exhaust requirements of the shroud's cooling system. Manufacturers MUST decide the most optimal perforation design and coverage, with optional I/O ports and the I/O shield structural integrity kept in consideration.
- Shroud Design: Baffles or channels MAY be used to optimize airflow over other heat-generating components such as system memory and VRMs
- Aerodynamic Shaping: Curves and fillets MUST be incorporated in the shroud design, whenever possible, to reduce turbulence and flow separation.

Note: A dedicated shroud MAY be omitted for low-power designs where the thermal solution requirements in Section 6.2 can be met without additional airflow guidance. In such cases, the compute node MUST still comply with all operating temperature limits in Section 6.1 when installed in a compatible enclosure.

7. Testing Requirements

To ensure interoperability, reliability, and performance across a wide range of components and deployment environments, all compute nodes conforming to this specification SHALL undergo testing aligned with industry-recognized standards for open and modular computing hardware.

7.1 Electrical Testing

Compute nodes SHALL be subjected to the following electrical tests to ensure user safety and insulation integrity:

7.1.1 Safety and Insulation Testing

- Dielectric Withstand Test (Hi-Pot Test)
    - Purpose: To verify the insulation strength of the compute node's components and PCB to prevent electrical breakdown and ensure safety.
    - Procedure: Applying a high voltage (AC or DC) between isolated parts for a specified duration and checking for current leakage or breakdown.
- Insulation Resistance Test
    - Purpose: To measure the resistance between isolated circuits to ensure effective insulation.
    - Procedure: Applying a DC voltage across insulation barriers and measuring the insulation resistance.
- Ground Continuity Test
    - Purpose: To verify the proper connection of all exposed metal parts to the ground terminal.
    - Procedure: Measuring the resistance between the ground pin and accessible metal parts (should be <0.1Ω).
- Standards Reference: IEC 60950 / IEC 62368-1.

7.1.2 Functional and Performance Testing

- Power-Up and Basic Functionality Test
    - Purpose: To ensure the compute node powers up correctly and basic I/O is operational.
    - Procedure: Apply 12VDC and verify power-on, power button function, and basic USB power.
- Voltage Rail Verification

    - Purpose: To confirm VRMs generate correct voltage levels within tolerance under various loads.
    - Procedure: Measure voltage at test points on the PCB.
- Ethernet Port Testing
    - Purpose: To ensure functionality and speed (2.5 Gbps or faster) of all Ethernet ports.
    - Procedure: Verify link establishment, perform data transfer, and run benchmarks.
    - Tools: Network testers, iperf.
- USB Port Testing (USB 2.0, USB-C, USB 3.0 Type A)
    - Purpose: To verify functionality and data transfer speeds of all USB ports.
    - Procedure: Test detection, power delivery (USB-C), and data transfer with various USB devices.
    - Tools: USB testers, data transfer benchmarks.
- DisplayPort Output Testing
    - Purpose: To ensure the DisplayPort output functions correctly.
    - Procedure: Verify signal output and resolution support with a compatible display.
- Front Panel Connector Testing (Power Button, Reset Button, Audio)
    - Purpose: To verify the correct operation of front panel connectors.
    - Procedure: Test power/reset button functionality and audio output.
- Signal Integrity Testing (High-Speed Interfaces)
    - Purpose: To ensure signal quality on 4C+ and 4C connectors for reliable data transfer.
    - Procedure: Measure signal parameters at the connector interface.
    - Tools: Oscilloscope, signal integrity tools
    - Considerations: May require custom test fixtures mimicking enclosure backplane.
- Power Integrity Testing
    - Purpose: To assess the stability and noise levels of power delivery.
    - Procedure: Measure voltage ripple, noise, and transient response.
    - Tools: Oscilloscope, power analyzer

7.1.3 Electromagnetic Compatibility (EMC) Pre-compliance Testing

- Conducted Emissions: Measure RF noise emitted through cables.
- Radiated Emissions: Measure RF noise radiated by the node.
- Electrostatic Discharge (ESD) Immunity: Test resistance to ESD events.
- Electromagnetic Interference (EMI) Susceptibility: Test operation in external electromagnetic fields.

7.2 Thermal and Environmental Testing

All OpenSFF compute nodes must undergo thermal validation under representative operating conditions to ensure reliable function and safety. Thermal tests are designed to evaluate the system's ability to maintain safe operating temperatures, prevent thermal throttling, and operate within acoustic boundaries. Tests must be performed using defined workloads and thermal conditions that simulate real-world deployment scenarios, including those with unfiltered airflow and exposure to airborne particulate matter.

OpenSFF-compatible systems are not required to meet formal ingress protection (IP) ratings; however, systems using open or semi-open airflow paths must demonstrate thermal resilience under controlled debris exposure conditions as defined in this document.

The following mandatory thermal and environmental tests MUST be performed:

7.2.1 Thermal Testing Under Specified Ambient Inlet Temperatures

- Purpose: To ensure the compute node can operate reliably without thermal throttling or component damage within the specified ambient inlet temperature range and under specific fan failure scenarios.

- Procedure: Run the compute node at its maximum TDP (120W as per Section 4.2) within a controlled environment with the following conditions:
    - Condition 1: All Fans Operational: Ambient inlet temperature maintained at ≤35°C with all enclosure cooling fans functioning correctly as intended by the enclosure specification. Monitor CPU/APU die temperature, memory module temperatures, and VRM MOSFET casing temperatures until steady state is reached.
    - Condition 2: Single Fan Failure: Ambient inlet temperature maintained at ≤35°C with a single non-operational cooling fan that is not directly cooling the tested node's active thermal zone (as defined by the enclosure's thermal design). Monitor the same component temperatures until steady state is reached.
- Pass/Fail Criteria:
    - CPU/APU Core Maximum Junction Temperature (Tj): ≤85°C
    - Memory Modules Maximum Junction Temperature: ≤85°C
    - VRM Mosfet Casing Temperature: ≤120°C
    - No thermal throttling of the CPU/APU or memory should occur during the test.

7.2.2 Thermal Performance Under Varying Ambient Temperatures

- Purpose: To evaluate the effectiveness of the cooling solution across the specified operating temperature range (10°C to 35°C).
- Procedure: Perform thermal testing (as in 7.2.1 - Condition 1) at different controlled ambient temperatures within the operating range.
- Analysis: Assess how component temperatures are affected by changes in ambient temperature and ensuring that the cooling solution remains adequate at the upper limit (35°C).

7.2.3 Transient Thermal Response Testing

- Purpose: To assess how quickly the thermal solution can dissipate heat when the workload (and thus power consumption) changes rapidly. This is important for real-world scenarios with fluctuating demands.
- Procedure: Apply a step load change (e.g., transitioning from idle to full load and vice versa) and monitor the temperature response of critical components over time. Measure the time constants for temperature rise and fall.
- Metrics: Rate of temperature change (°C/second), overshoot, and settling time to reach a stable temperature.

7.2.4 Hot Spot Identification

- Purpose: To identify any localized areas of excessive heat on the compute node PCB or components.
- Procedure: Use infrared (IR) cameras to create thermal images of the node under load, highlighting areas with the highest temperatures. This can help identify potential design flaws or areas needing improved cooling.

7.2.5 Acoustic Testing Under Thermal Load

- Purpose: To measure the noise levels generated by the cooling system (enclosure fans) when the compute node is under high thermal load (80-90% of system TDP). This is important for user comfort, especially in desktop environments.
- Procedure: Measure sound pressure levels at a specified distance from the enclosure while the compute node is running a demanding workload that causes the fans to operate at higher speeds.
- Metrics: Noise levels in dBA.

7.2.6 Long-Duration Thermal Soak Test

- Purpose: To assess the long-term reliability of the thermal solution and components under continuous thermal stress.
- Procedure: Run the compute node at a high load within the maximum ambient temperature for an extended period (e.g., 24-72 hours) and monitor for any signs of thermal degradation or failure.

7.2.7 Debris Exposure Validation

- Purpose: To validate system thermal and mechanical resilience in environments where unfiltered airflow introduces particulate accumulation over time. The test assesses whether thermal management systems (e.g. heatsink or equivalent thermal solution, shroud) continue to perform within specification after sustained exposure.
- Procedure: See details below.
    - Setup: System configured in a standard operational chassis with airflow paths unobstructed, and placed inside a test chamber to simulate an ISO 14644-1 Class 9 cleanroom. Airflow is directed through natural intake zones using an external fan array integrated into the chassis.
    - Debris Composition: ISO 12103-1 A2 Fine Test Dust or equivalent used as a particulate source.
    - Exposure Method: Dust is aerosolized and introduced into the airflow path in intervals over a 72-hour simulated uptime period. The quantity SHALL be in accordance with the ISO Class 9 cleanroom specification.
    - Thermal Load: The compute node must run a sustained high-load thermal stress equal to 80-90% of total system TDP throughout the exposure window.
    - Monitoring: Record inlet and outlet temperatures, fan RPMs, and internal sensor telemetry (CPU, DIMM, VRMs, and other sensors).
- Validation Criteria: See details below.
    - No CPU/APU system throttling observed during or after the test
    - No increase in maximum fan RPM exceeding 10% over baseline
    - Acoustic measurements must remain within 3 dBA of pre-test levels
    - Post-test visual inspection must show no critical obstructions that may impair serviceability or airflow.

7.3 Mechanical Testing

7.3.1 Vibration and Shock

Each compute node must satisfy all applicable shock and vibration standards as outlined in IEC 60068-2-57:2013 and EC 60068-2-81:2003. During operational shock and vibration testing, the nodes MUST maintain continuous electrical performance with no interruptions. For non-operational testing, physical damage or limitation of functional capabilities MUST NOT occur to the nodes.

	Operating	Non-Operating
Vibration	0.5 G RMS, 5 to 500 to 5 Hz Random Vibe, 1 sweep, 20 min along three axes (+/–) 5–20 Hz – 6 dB/Oct 20–250 Hz – 0.0007 G²/Hz 250–500 Hz – 6 dB/Oct	1.2 G, 5 to 500 to 5 Hz per sweep 1 sweep at 0.5 Octave/min, 3 axes 5–10 Hz – 0.5 G 10–350 Hz – 1.2 G 350–500 Hz – 0.5 G

TABLE 7.3.1 Vibration and shock requirements

7.3.2 Mechanical Compliance of SFF-TA-1002 Interface

The compute node’s plug, based on the SFF-TA-1002 connector specifications, SHALL meet the mechanical performance requirements defined in this section to ensure interoperability and reliable engagement with the corresponding backplane connector.

Mechanical testing SHALL be conducted using an axial tension/compression system (e.g., Instron Tensile Tester) in accordance with EIA-364 procedures. All force measurements SHALL be executed at a constant rate of 25.4 mm/min. Testing SHALL be performed using compute nodes manufactured to this document's upper limits, as specified below, to represent worst-case tolerance conditions.

Mechanical Test	Procedure	Test Description
Insertion Force (Compute Node to Backplane Connector)	EIA-364-13	Measure axial insertion force required to fully engage the compute node into the backplane connector.
Unmating Force (Compute Node from Backplane Connector)	EIA-364-13	Measure axial force required to disengage the compute node from the backplane connector.
Durability (Mating/Unmating Cycles)	EIA-364-09 (Modified)	Plug and unplug the compute node at a controlled rate of 25.4 mm/min. Perform required cycles for connector grade per the table below. Replace the backplane connector after every 25 cycles.

TABLE 7.3.2a Mechanical testing requirements

Connector Grade	Number of Cycles
A	200
B	100
C	50

TABLE 7.3.2b Mating cycles by connector grade

7.4 Compliance Testing

Final verification SHALL be conducted by accredited laboratories to confirm conformity with all requirements specified in Section 8, including:

- EMC emissions and immunity
- Electrical safety and insulation
- Environmental directive compliance

8. Compliance and Certification

8.1 Electromagnetic Compatibility (EMC)

- **FCC CFR47 Part 15, Subpart B, Class A criteria:** U.S. regulation for controlling electromagnetic interference from digital devices.
- **EU EMC Directive (2004/108/EC):** Establishes uniform EMC requirements across EU member states, ensuring mutual acceptance of compliant equipment.

8.2 Safety Standards

- **UL 62368-1, IEC 62368-1, EN 62368-1:** Hazard-based safety standards for audio/video, information, and communication technology equipment.

8.3 Environmental Standards

- **RoHS Directive (2015/863/EU):** Restricts use of specific hazardous substances in electrical and electronic equipment to protect human health and the environment.
- **REACH Regulation (EC) No 1907/2006:** Requires registration, evaluation, authorization, and restriction of chemicals within the EU.
- **WEEE Directive (2012/19/EU):** Aims to reduce the environmental impact of electrical and electronic equipment through proper waste handling and recycling.

9. Usage of the OpenSFF Name, Trademark, and Associated Symbols

9.1 Usage

OpenSFF holds various copyrights and trademarks in the US, Europe, and other jurisdictions, including the OpenSFF name, logo, and related marks. These intellectual property assets are intended to signify compliance with the OpenSFF specification suite and to ensure interoperability, trust, and consistent implementation.

Use of the OpenSFF name, logos, or associated symbols is subject to a non-exclusive, revocable license that may be granted to manufacturers, system integrators, or other stakeholders who meet the criteria set forth in this specification and any associated OpenSFF documents.

9.2 Compatible vs Certified

“OpenSFF Compatible” means the product adheres to relevant portions of the OpenSFF Compute Node Specification but has not undergone formal compliance testing by OpenSFF or a designated certification body.

“OpenSFF Certified” means the product has successfully completed formal compliance and interoperability testing under the OpenSFF certification program. Only certified products may use the OpenSFF Certified logo.

Manufacturers MUST NOT use the terms *OpenSFF Certified* or display associated certification marks unless explicit, written approval has been granted by OpenSFF or its designated testing and certification authority.

9.3 Usage of the Logo and Name on Packaging

The OpenSFF logo and name MAY be used on product packaging, datasheets, or marketing materials ONLY IF the product is either certified or clearly labeled as compatible. The logo must appear in accordance with OpenSFF’s Brand Usage Guidelines, which specify:

- Minimum clear space and sizing requirements
- Approved color palettes and background usage
- Restrictions against modifying the logo’s shape, text, or orientation

Misuse of the OpenSFF logo or name may result in revocation of trademark privileges and/or legal action.

9.4 Permitted Versions

To ensure consistency, compatibility, and forward-compatibility, the following versioning policy applies:

- New Development: All new products or significant redesigns SHOULD use the latest published

version of the OpenSFF Compute Node Specification (including the most recent errata or revision).

- Legacy Designs: Products built to previous versions MAY continue to be manufactured and sold without change.
- Modified Designs: If a manufacturer modified a product built to an earlier version, the updated product MUST be updated to the latest applicable version of the specification.

OpenSFF reserves the right to deprecate specific versions or clarify errata in a manner that requires reevaluation of compatibility status.